Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-8. (Cancelled)

Claims 9-16. (Withdrawn)

17. (New) A hardware-based multithreaded processor comprising:

a plurality of microengines, each of the microengines supporting instructions that perform an arithmetic logic unit (ALU) operation on one or two operands, deposit a result in a destination register and update ALU condition codes according to the result; and

a local register instruction that loads one or more bytes within a local register with a shifted value of another operand.

18. (New) The processor of claim 17 wherein the destination register is an absolute transfer register.

19. (New) The processor of claim 17 wherein the destination register is a context-relative transfer register.

20. (New) The processor of claim 17 wherein the destination register is a general purpose register.

21. (New) The processor of claim 17 wherein the local register instruction comprises the destination register.

22. (New) The processor of claim 17 wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes are affected.

23. (New) The processor of claim 22 where in the mask is 4-bits.

24. (New) The processor of claim 22 wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded.

25. (New) The processor of claim 17 wherein the local register instruction comprises a context relative source register.

26. (New) Apparatus comprising:

in a hardware-based multithreaded processor comprising a plurality of microengines, each of the plurality of microengines including a command that causes an arithmetic logic unit (ALU) to load one or more bytes within a destination register of a selected microengine with a shifted value of another one or bytes of a source register.

27. (New) The apparatus of claim 26 wherein the command comprises a field representing a mask that specifies which byte or bytes are affected.

28. (New) The apparatus of claim 27 where in the mask is 4-bits.

29. (New) The apparatus of claim 27 wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded.